

EDA tools focus on IC optimisation

Athena Design Systems

(www.athenadesign.com) has been concentrating on delivering tools that can achieve design closure and meet the physical implementation challenges of complex nanometer chip design since it was founded in 2003.

For devices manufactured at 90nm and lower processes to meet market windows with lower costs and higher yields, chips have to be optimised to achieve reliable and quicker design closure. This includes timing management and signal integrity, both of which are affected at the lower nanometer scales.

It is estimated that each new process node doubles design time spent on back-end IC design, tripling development costs with verification and manual intervention to 'fix' conflicting design constraints. This can be costly on large, complex designs, which by definition have more data to process to solve these issues. At 90nm and below, the IC implementation flow requires serial execution of analysis and extraction tools in batch mode to locate timing, signal integrity, power and manufacturability problems. However, serial engineering and processing has been cited as a cause of bottlenecks in analysis and design change management. These

bottlenecks can lead to an undue level of time being spent on manual optimisation of the physical chip design. Automating and managing this can speed a chip's critical routing.

Athena has introduced what it claims is the industry's first concurrent analysis and optimisation system for managing deep-sub-micron effects. It is based on the company's optimisation algorithms, embedded analysis and extraction engines and its patented multi-processing and tiling technologies. The idea is to provide a central point of control from which designs can be explored and the physical layout optimised. It also allows the consequences of changes to be evaluated to reduce the risk of problems later in the design flow. The system architecture includes a design management infrastructure that manages the optimisation tasks transparently. It can be used with IC design flows and routers from major EDA vendors.

Founders John Murphy, the CEO, and CTO Dimitris Fotakis both worked at Cadence. Fotakis was also the founder of AmmoCore Technology. The company's IC optimisation tools have been developed with NEC Electronics, integrated device manufacturers and fabless semiconductor companies for the last two years.

Cryptographic devices boost wireless security

Wireless is all around, but the applications are prone to security breaches. The IEEE has been working towards standardising security levels for wireless designs. As a lot of legacy equipment is still in use, interoperability requires cryptographic engines that support the DES (Data Encryption Standard) and AES (Advanced Encryption Standard).

Bristol-based PicoChip (www.picochip.com) will use Elliptic Semiconductor's (www.ellipticsemi.com) cryptographic co-processor engine for its PC202, PC203 and PC205 PicoArray processors, used in fixed and mobile WiMAX, W-CDMA, 802.16d wireless applications.

One interesting aspect of this application, jointly defined

by the companies, allows PicoChip to design according to compliance with legacy equipment and standards that are not yet ratified. The Elliptic encryption device allows the PicoArray chips to support W-CDMA and WiMAX in the same device, as well as IPsec for home basestations.

