

There's an attractive conceptual simplicity to single-chip systems, in which everything from memory arrays and digital signal processing to RF front ends and high-speed wireline interfaces are melded onto a piece of silicon. It's on one piece of silicon – a system-on-chip (SoC) – so it must be cheaper and simpler to use. However, the reality is that it may be better to use different chips for different functions and just make it look as though everything is in one piece, by putting them all into a multichip module, or, as the current fashion dictates, a system in package (SiP).

The question for engineering managers is how to decide whether to go for the SoC or SiP integration path. At one level the answer is easy: with advanced SoC designs costing around \$30m and SoC start-ups spending up to \$80m developing their product line before reaching profitability, the SoC route is only open to companies that see the chance to sell hundreds of millions of dollars of the resultant chips. SiP techniques, however, can provide SoC-style integration to smaller markets and bring other benefits, such as reducing supply chain risk by having multiple sources for critical parts of the final SiP.

Bryan Lewis, research vice president and chief analyst



question is, should we keep doing SoCs or is it time to move to SiPs?" he asked.

Yazdani said CMOS is significantly cheaper for integrating a large number of digital functions, but that when you add large quantities of dynamic or non-volatile memory and other technologies the price curve goes up and it becomes more difficult to justify the SoC. At lower volumes, SiP has a greater chance because the development costs are lower.

Chris King is president and CEO of AMI Semiconductor, which produces chips that go into extreme environments. She said: "We have to optimise whether we produce an SoC or an SiP based on our design point. So, depending on what we want in terms of function, cost, power, and performance will determine what we choose," she said. "When we use a mainstream technology like CMOS, those sorts of designs tend to converge on an SoC. When we are integrating a very diverse set of technologies we go for a SiP implementation."

#### DESIGN DEMANDS

King said that when the design has to work in a very robust environment, such as driving 80V in an automotive or industrial application, AMI tends to choose separate analogue and digital chips. Such applications tend to have

**System-in-package looks to be an attractive option for projects that cannot justify a system-on-chip approach. But people working with them say there are many obstacles still to be overcome before it becomes mainstream.**

# Silicon sandwich

by Luke Collins

at Gartner Dataquest, moderated a panel discussion on making the choice between SoC and SiP at the Globalpress Electronics Summit in Monterey, California, in March. He said the market for 'second-generation' SoCs, which have multiple processor cores each driving a subsystem with its own operating system and application software, would be worth \$30bn by 2010. The SiP market would be worth a quarter of that, he said, but would be growing more quickly.

Jim Walker, research vice president of Gartner Dataquest's semiconductor manufacturing team, said the advantages of an SoC included its high performance and integration, long product life and suitability for large volumes. These advantages have to be balanced by issues such as the high cost of the silicon, how much it costs to design and test, and what will probably be lower per-die yields because they are larger devices. SoCs will also tend to take longer to get to market, be more complex to use if they need to handle both analogue and digital signals, and may bring concerns about intellectual property.

Walker defined an SiP as a functional building block containing multiple die and possibly discretised in one semiconductor package. Its key advantage is adaptability, he said, as the approach is appropriate for low or high volumes, and can handle mixed die and process technologies. SiP designs should also have lower development and non-recurring engineering (NRE) costs than SoC approaches. Among the disadvantages Walker listed were the cumulative yield losses involved in linking the many devices that make up an SiP, lower performance, and the availability or otherwise of known good die.

"But it's inherently obvious that SiP wins most of the time," Walker claimed.

SiP is winning in what might seem to be the most unlikely places. The cellphone market, which demands integration and offers extremely high volumes, may seem like the definitive market for SoCs. But, according to Walker, Motorola's Razr phone includes five SiPs and 10 multichip packages.

Scott Jewler, chief strategy officer of Stats ChipPac, which provides the packages for both SoC and SiP devices, said that 85% of SiPs are used in cellphones and telecoms equipment, because of their short product lifetimes. It can be a matter of months for a cellphone. The use of SiPs has enabled companies to add incremental features such as MP3 players and cameras very quickly.

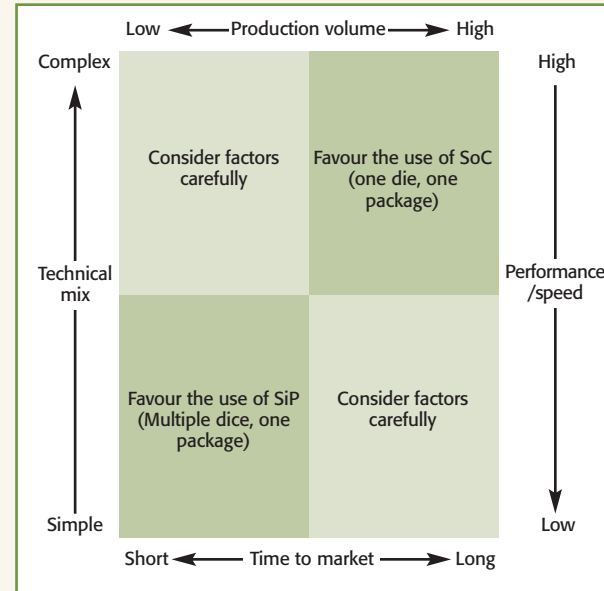
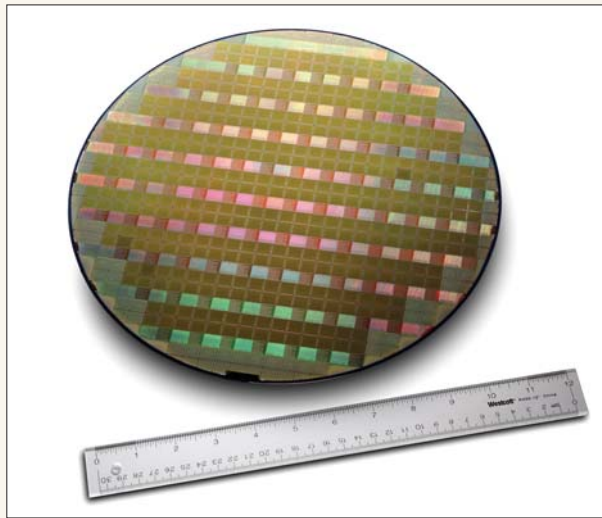
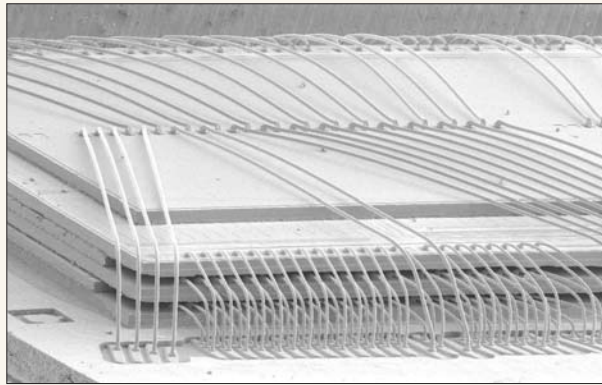
"That is what has enabled SiP to get into volume production," claimed Jewler.

Other key markets for SiP include in RF power amplifiers, analogue front-end modules, transceivers, and low-noise amplifiers. In consumer electronics, SiPs are used in DC/DC converters, broadband modems and fingerprint sensors, as well as in wireless-networking equipment. SiPs also appear in memory cards and games packs, as well as in Bluetooth, Wi-Fi and Global Positioning System cards.

Mobashar Yazdani manages ASIC programmes for computer maker HP. He spends his time trying to make the best trade-offs for each design he is asked to do. "The

other requirements too, such as the need for very high electrostatic discharge protection and strong electromagnetic compatibility compliance, or the integration of sensors, which also drive the designer towards an SiP solution. Low-power designs or precision analogue circuits would also push the choice towards SiP. Kings said cost is another factor driving the use of SiP, for example when the design needs to integrate memory and intelligence with analogue circuits.

King gave the example of two designs for washing machine controllers. An SoC implementation included an 8051 microcontroller, flash memory, high-voltage interfaces, analogue to digital converters and other circuits. It took 24 months to get to production and had an average selling price of \$2.40. When the client wanted a controller for a more complex washing machine, with a 16bit microcontroller and more flash memory, it was more economical to produce an SiP. That part took 18 months to get to production and had an average selling price of \$4. "The →



Matrix showing the areas into which SoC and SiP implementations fit most readily

system. By integrating a processor into your platform you suddenly have thousands and thousands of wires that can connect directly into the processor's databus and register files. With that bandwidth capability you have another dimension for improving performance, and I see that as another reason why you integrate."

Bolsens said integrating more functions on chips such as FPGAs is making the problem really complex, which is why it costs hundreds of millions of dollars to develop such platforms. "That's what SiP has the potential to solve in the future, breaking that exponential dependency on complexity. So SiP will make SoC capabilities available to the 'have-nots' of deep sub-micron SoC.

"There are two things that are needed to meet this vision. One is advanced SiP technologies that can give the bandwidth of SoC, with tens of thousands of interconnects. The second is a substrate on which you are willing to build these SiPs and that's where I see a future for FPGAs. I would like to position FPGAs as a virtual backplane to allow you to build specific applications on top of a programmable interconnect to meet the capabilities and leverage the bandwidth," Bolsens proposed, adding that routing signals through the programmable interconnect of an FPGA within an SiP would provide flexibility without the energy cost of doing the same to FPGAs mounted separately on a printed circuit board.

"The virtual backplane is a long-term vision," said Bolsens, adding that it is important that the industry lines up behind it to make it happen.

Despite the apparent temptations of using SiP in favour of SoC, there are problems. Yazdani explained: "One of the things that is lacking here is the tools, which need to be



worked on to make SiP a reality. There are two types of tools, for design composition and concurrent design, and a lot is happening on the concurrent tools. We need to be able to do trade-offs of different SiP forms. You want to make the decision yourself rather than have your fabless guys saying: 'this is how you go'."

**DIFFICULT INTEGRATION**

King agreed: "The challenges in SiP design are a little more difficult than in SoC design. For SiP we need design tools not only for the electrical rules but for mechanical rules as well. It would be great if we could have more software in terms of optimising SiP versus SoC.

"The question is, who is going to invest in the tools improvement we need for SiP, and who has the economic opportunity to invest in the tools and get the return on that investment?"

Even if they are easier to design, a problem for SiP integrators is making sure that there are easy ways of getting them from the drawing board into volume manufacture, particularly when it is likely to be smaller companies who find they have to take the SiP rather than the SoC path. Bolsens said: "The big challenge is the business challenge. You have to have all players in the chain lined up, from the foundry to the EDA companies to the system houses that are developing architectures that can leverage SiP capabilities. That is the key barrier to having this vision come true."

Jewler added: "The big companies have the advantage in SoC. But I think there are a lot of medium to smaller companies that have valuable IP. SiP provides a viable solution for them to bring it to market. The challenge remains in the supply chain and how it works. The technical packaging issues are being resolved. The final test, supply chain and business models continue to evolve."

Chris King said AMI would sell bare die, but that customers are looking for solutions so she would consider buying dice from other companies and managing the integration of them. She said AMI would establish multiple

sources for the other components to reduce risk. Martino said IBM would take a similar approach.

Bolsens said: "In the end the customer has to benefit from the right business model. The problem with selling dice and bringing dice together in a package SiP is the accumulating multiple margins."

Yazdani said that SiP customers might be able to deal with a single supplier; but still need to talk to many partners to solve the engineering issues.

Martino said: "A key part of this will be partnerships, open platforms and standards that enable a number of companies to build on a given capability, not a single company coming with a single solution."

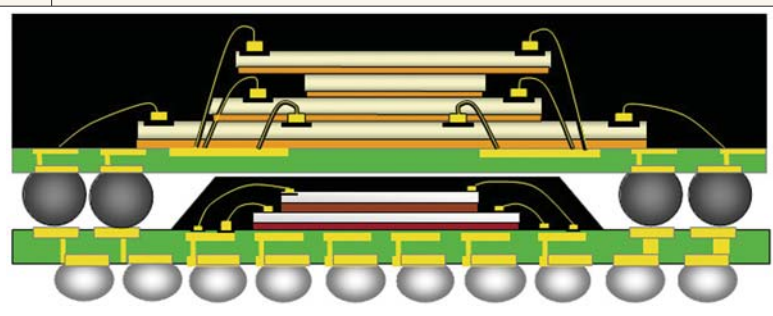
Bolsens claimed standards would play a role in driving SiP acceptance: "I think we will only really see the success of SiP if people start designing with SiP in mind. Standards are important if people can agree on what it means to design for SiP and take it into account from the start."

King said: "Standards are nice but difficult. When an SiP is optimised we're talking about integrating so many technologies from so many sources. I think it would be great to do that, but I think it will be difficult because there are so many variables in the equation"

Bolsens countered: "If standards don't happen I think SiP will always have a hard time competing with SoC."

It may look attractive as an option, but SiP as a technology has a long way to go before it breaks out of the huge-volume applications that have driven it so far. ■

**“If standards don't happen I think SiP will always have a hard time competing with SoC”**



Stacked chip packages (top and above) can become quite complex, allowing many chips to be placed in one package. Although assembly can be complex, the final system cost may still be lower than using large, monolithic dice straight off a wafer (above middle).

higher complexity application drove us to use SiP," King said.

Ron Martino, director of Power architecture products, systems and technology group at IBM said the company had a range of choices over which path it takes for each product. "But there are a number of capabilities for which SoC is critical," he said.

Xilinx relies on SoC technologies for its FPGAs, which can include embedded processors, embedded memory and fast transceivers.

Ivo Bolsens, chief technology officer, said: "One of the key reasons for this [reliance] is bandwidth within the



Motorola's Razr phone uses system-in-package devices

Luke Collins is a freelance technology journalist