

FPGAs break \$2/100k gate bar

Claiming to deliver the lowest cost per logic cell in the FPGA industry, Xilinx (www.xilinx.com/spartan3e) announced the fourth family in its Spartan family, priced at \$2.00 for 100k system gates. The Spartan-3E also has a unit cost of \$10.00 for devices over 1 million system gates.

The announcement, at this year's Globalpress Electronics Summit, was appropriate to the conference's theme, **The era of convergence** as the flexibility of FPGAs is becoming increasingly important as standards and protocols are ratified and adopted for high-speed, wireless, data, voice and video transmission.

At this price point, the Spartan-3E is expected to be used in consumer applications, significantly in flat panels TVs as the industry moves from analogue to digital broadcasting yet standards are still being defined. As standards evolve, FPGAs enable systems to be upgraded without replacing whole tracts of equipment. They are also for use in prototyping, networking, communications and industrial electronics. Consumer electronics is a significant market sector for convergence. Wim Roelandts, Xilinx's president and CEO, confirmed that 20 per cent of the company's revenues are from consumer electronics, increasing from 15 per cent three years ago.

A standard Spartan-3E device implements microprocessor, microcontroller and DSP functions. The 32bit MicroBlaze and the 8bit PicoBlaze embedded processors can be included for an effective cost of \$0.48 and \$0.10 respectively, claims the company.

Whereas programmable devices were once used as glue logic, now the need for gates and routing as well as DSP means they are popular in the consumer space. The Spartan-3 family was introduced for I/O-centric designs, with a dual pad ring for I/O, increased the I/O available. This latest addition to the Spartan family, has less I/O than Spartan but more logic for gate-centric designs. There is support for 18 common I/O standards, including PCI 64/66, PCI-X 100, RSDS and mini LVDS as well as interfaces to DDR memories. With these platform features being in-built, the number of other discrete devices needed is reduced, lowering overall systems costs and simplifying design. SPI and byte-wide parallel flash memory, for configuration support, also lower system costs.

As standardisation of protocols and platforms is put in place the ability to dynamically reconfigure and to keep standards in a memory to be downloaded when needed, will decrease the time to market for products. In a sector, where one to two million units is considered medium volume, this ability to put products on shelves could be the difference between market share and 'me too' products.

First shipments of the Spartan XC3S100E, 100k system gate device are with customers and all five devices in the pb-free packaged family will be in volume production in the second half of this year.

Although Spartan-3E uses 90nm process technology, Roelandts predicts 65nm devices in the next two years for Spartan devices.

The Xilinx ISE (Integrated Software Environment) 7.1i tools provide software support. This latest release of the tools has integration and speed elements and new power analysis, hierarchical design, simulation and debug features.

It supports Linux-based design environments and the company's Virtex-4 platform FPGAs.

