

Wafer shift promises cheaper chips for some

THE SEMICONDUCTOR manufacturing industry is poised to get some cost relief thanks to a shift to denser processes and bigger wafers. But the trend remains towards increased collaboration as the underlying pressures of staying on the Moore's law curve increase.

Edward So, vice president and director of California technology and manufacturing, Intel, is confident that the industry can remain on the Moore's law scaling curve for the next 10 years at least, and remain economic. "Over the last 30 years the cost a transistor has declined 30-35% per year, or more than twofold every two years. That's six orders of magnitude over 30 years," he said.

He said that, 10 years ago, an economically optimal fab cost \$1bn and produced 20,000 wafer starts per month, using 200mm wafers. Today's equivalent uses 300mm wafer, costs \$3bn and produces 30,000 wafer starts per month. But each 300mm wafer can carry more than twice the

number of chips than a 200mm wafer.

"The 300mm fab turns the clock back 10 years to allow us to compensate for process complexity," So said. "Economy of scale is playing a bigger role now."

Others said they believe economies of scale should come through collaboration to tackle hard problems, rather than consolidation. Gregg Higashi, chief technology officer of Applied Materials, said that traditional transistor scaling is running out of steam: "It used to be all about scaling geometries, but now gate leakage currents are scaling exponentially."

The industry's response has been to look at new techniques such as ultra-shallow junctions, shallow trench isolation, strained silicon and new materials to help with scaling. This has introduced complexity, which Higashi says requires better co-operation in all parts of the food chain to enable new processes to be delivered in a manufacturable way.

Designers, tool and equipment vendors and manufacturers also face an increasing challenge as statistical process variation becomes more important to chip designs as minimum dimensions shrink.

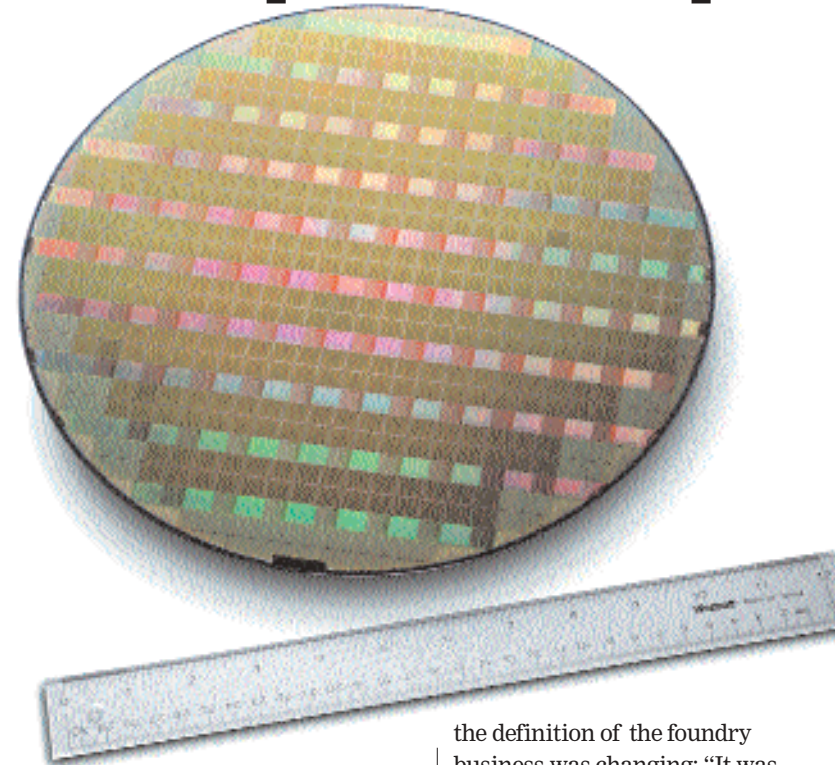
"It's a very important issue as we migrate to design and process matching," said Shih-Wei Sun, senior vice president of central research and development at foundry company UMC. He says EDA vendors will be in the middle of this issue and that collaboration will be very important to handle this "monumental challenge".

Julie England, vice-president and business manager for the Sun Microsystems business of Texas Instruments, sees the issue as providing an opportunity for process-technology design-tool vendors, as manufacturers look for ways to squeeze costs and time out of their processes.

Vincent Tong, vice-president of product technology in the advanced product group at Xilinx, said Field-Programmable Gate Arrays (FPGAs) can help manage process variations because they allow the creation of test structures on the fly. For example, the FPGAs can be programmed to act as thousands of ring oscillators during test, which can be used for real-time data gathering on the process.

"It's why the FPGA is such an effective vehicle for critical dimension control," he said. But the tool is only useful if it is applied, which is why Xilinx is working ever more closely with its foundry partner UMC. "At 90nm we engage with UMC when it is buying the fab equipment. [It is about] understanding the transistor structures early enough to do design with them."

Equipment vendor Applied is taking a similarly collaborative approach to tackle statistical process variations. Higashi said



Applied worked with Toshiba on an analysis of the sensitivity of a process to its implant and rapid thermal annealing steps. The analysis found that the most sensitive factor to control was the processing temperature, and that they had to improve their control threefold.

"We figure out what the spec has to be and then go make it work," Higashi said.

Jackson Hu, CEO of foundry company UMC, questioned whether



Shih-Wei Sun

the definition of the foundry business was changing: "It was originally defined as cost-effective manufacturing but the gap in process technology with the IDMs [integrated device manufacturers] is narrowing and at 90nm, the foundries may be ahead."

UMC research chief Shih-Wei Sun said that IDMs had the benefit of tailoring their processes to match their designs, which foundries cannot do. He called for more collaboration "which may include exchanging process nodes with IDMs."

The race to even denser processes continues unabated, even as 90nm reaches production. "We're planning for a two-year pace of [process migration] and we are just at the beginning of what people can do with SoC," said England. "At 65nm, it opens up a whole new world. The pressure is on us to extend bulk CMOS and keep the costs down so people can use it."

"We're on the verge of a billion transistors on a chip, which gives our customers a world of opportunities."

UMC's Hu said: "We can produce prototypes for 65nm in the second half of 2005, with production in 2006."

The race to denser processes doesn't stop there. "The investments are in place to start moving in the 45nm direction," said Higashi of equipment vendor Applied. Intel, TI and UMC all said they had 45nm processes in development.

"TI has 65nm processes in the oven and 45nm is in development," said England.

Intel's So said 45nm processes may need EUV lithography, along with high-k gate dielectrics and metal gates. Sun says UMC is trying to use phase-shift lithography for the critical layers of 45nm, to delay the need for extreme ultraviolet lithography.

England said: "The convergence of three [changes in process technology] at one major node is what is scaring me the most." But she said there is a convergence happening in the industry, with all the major vendors heading in one direction, rather than taking on a radical new transistor design.

Yet, despite the professed need to work together to tackle difficult common problems that threaten the industry's future, collaboration can break down. Intel recently announced it had chosen the high-k dielectric and metal-gate materials that would help it overcome gate leakage problems, and was keeping them secret to gain a competitive advantage.

"The high-k dielectric work was collaboration well in advance [of production] with Sematech," said So. "There are pre-competitive stages where you work closely to narrow the options. But once you move into competition you want to have your own IP and then go as fast as you can."